Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An information reproducing apparatus, which supplies a read signal reproduced from a recording medium to a maximum likelihood decoding means, and decodes and reproduces a data, comprising:

a clock source for supplying a clock signal to the maximum likelihood decoding means;

clock control means interposed between the clock source and the maximum likelihood decoding means; and

a controller for controlling an operation mode such as decoding or the like,

the clock control means supplying the clock signal to the maximum likelihood decoding means in only decoding,

the clock control means including:

a clock driver;

switching means provided on a pre-stage of the clock driver; and

two logical product circuits provided on a pre-stage of the switching means,

wherein the clock signal is supplied in common to the two logical product circuits.

2. (Original) The information reproducing apparatus according to claim 1, wherein the maximum likelihood decoding means is a Viterbi decoder.

3. (Original) The information reproducing apparatus according to claim 2, wherein when the maximum likelihood decoding means is a Viterbi decoder, waveform equalization means for the read signal is provided on a pre-stage of the Viterbi decoder.

4. (Original) The information reproducing apparatus according to claim 3, wherein the waveform equalization characteristic is a partial response characteristic.

5. (Original) The information reproducing apparatus according to claim 4, wherein a PR (1, 2, 1) characteristic is used as the partial response characteristic PR.

6. (Original) The information reproducing apparatus according to claim 4, wherein a PR (1, 3, 3, 1) characteristic is used as the partial response characteristic PR.

7. (Currently Amended) An ~~The~~ information reproducing apparatus ~~according to claim 2~~, which supplies a read signal reproduced from a recording medium to a Viterbi decoder, and decodes and reproduces a data, comprising:

a clock source for supplying a clock signal to the Viterbi decoder;

clock control means interposed between the clock source and the Viterbi decoder; and

a controller for controlling an operation mode such as decoding or the like,

the clock control means supplying the clock signal to the Viterbi decoder in only decoding,

wherein the Viterbi decoder ~~is composed: of~~ includes:

a branch metric circuit for calculating a branch metric from a read signal;

an adder-comparator-selector circuit for adding the branch metric and a path metric, and selecting a transition state; a status memory block for holding a selected status data; and

a data merge block for decoding the read signal from the status data.

8. (Original) The information reproducing apparatus according to claim 1, wherein the read signal is a signal from a magneto-optical disk.

9. (Original) The information reproducing apparatus according to claim 1, wherein the clock source is a PLL circuit to which the read signal is supplied.

10. (Canceled)

11. (Currently Amended) An ~~The~~ information reproducing apparatus ~~according to claim 10~~, which supplies a read signal reproduced from a recording medium to a maximum likelihood decoding means, and decodes and reproduces a data, comprising:

a clock source for supplying a clock signal to the maximum likelihood decoding means;

clock control means interposed between the clock source and the maximum likelihood decoding means; and

a controller for controlling an operation mode such as decoding or the like,

the clock control means supplying the clock signal to the maximum likelihood decoding means in only decoding,

the clock control means including:

switching means provided on a pre-stage of the clock driver; and

two logical product circuits provided on a pre-stage of the switching means, wherein the clock signal is supplied in common to the two logical product circuits, and

wherein a read gate signal obtained from the controller is supplied to a first logical product circuit of first and second logical product circuits, and a control signal indicative of a power saving mode state and generated by the controller is supplied to the second logical product circuit and the switching means.